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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,992	04/21/2004	Jerome Bombal	TI-35112	5501

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,992	BOMBAL, JEROME	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Gorman et al., US PG Pub 2004/0218454.

3. With respect to claim 1, Gorman teaches an electronic device, comprising:

a memory structure comprising an integer M of memory word slots, wherein each memory word slot is operable to store an integer N of bits, in fig. 1, SRAM 110, and described in par. 37.

a scan storage circuit, operable to receive a scan word having a number of bits less than MxN, in par. 6, as well as par. 37. It is disclosed therein that one "fuse word" is scanned in at a time, which is equal to the width of the SRAM array, N.

control circuitry for causing successive scan words to be written into the scan storage circuit, for causing successive scan words to be written from the scan storage circuit into the memory structure, and for causing successive scan words to be read from the memory structure into the scan storage circuit, in par. 37.

4. With respect to claim 2, Gorman teaches the electronic device of claim 1 wherein the scan storage circuit is operable to receive a scan word consisting of N bits, in par. 6, as discussed above.

5. With respect to claim 3, Gorman teaches the electronic device of claim 2 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit, in par. 39.

6. With respect to claim 4, Gorman teaches the electronic device of claim 3 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as corresponding successive scan word is written into the scan storage circuit, in par. 7.

7. With respect to claim 5, Gorman teaches the electronic device of claim 4 wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in parallel, in par. 7.

8. With respect to claim 6, Gorman teaches the electronic device of claim 5:

wherein the successive scan words to be written into the scan storage circuit comprise a test sequence, in par. 6; and

further comprising circuitry for comparing the successive scan words to be read from the memory structure to the test sequence, in par. 6.

9. With respect to claim 7, Gorman teaches the electronic device of claim 6:

wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells, in par. 6; and

wherin each set of N memory cells comprises N latches, in par. 6.

10. With respect to claim 8, Gorman teaches the electronic device of claim 6 wherein each of the N latches comprises:

a first inverter having an input providing an input to the latch and an output providing an output of the latch; and

a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch, because this is the definition of a latch. It is inherent that the Gorman reference teaches such a latch.

11. With respect to claim 9, Gorman teaches the electronic device of claim 7 wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells, in par. 6; and

wherein each set of N memory cells is operable to store incoming data without responding to a clock transition, in par. 39.

12. With respect to claims 11-13, Applicant claims the same electronic device as claims 2-5 but dependent on claim 1, and are therefore rejected using similar logic.

13. With respect to claim 14, Applicant claims the same electronic device as claims 4-5 and is therefore rejected using similar logic.

14. With respect to claims 15-16 Applicant claims the same electronic device as claims 7-8 and is therefore rejected using similar logic.

15. With respect to claim 17, Gorman teaches the electronic device of claim 1 wherein the memory structure, the scan storage circuit, and the control circuitry are all in a single integrated circuit, in fig. 1.

16. With respect to claims 18-20, Applicant claims a method of operating an electronic device that corresponds the electronic device of claims 1-3 and is therefore rejected using similar logic.

17. With respect to claim 21, Gorman teaches the method of claim 19 and further comprising causing each successive scan word to be serially read by shifting bits out from the scan storage circuit during a same time period as causing corresponding successive scan words to be serially written by shifting bits into the scan storage circuit, in pars. 6-7.

18. With respect to claim 22, Applicant claims a method that corresponds to the electronic device of claim 5 and is therefore rejected using similar logic.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gorman as applied to claims 1-9 and 11-22 above, in view of Colon-Bonet, US Patent 6,970,897.

22. With respect to claim 10, Gorman teaches all other limitations of the parent claims but fails to disclose the width of the data circuit. Colon-Bonet teaches a system where the wherein the width N of an electronic device is selected from a group consisting of 128, 64, 32, 16, 8, and 4, in col. 6, lines 47-49.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to combine the electronic device of Gorman with the electronic device of Colon-Bonet to have a width N of 128, 64, 32, 16, 8 or 4 because it is widely known that a word width is selected from the group of numbers that are powers of two, and by selecting a value between 4 and 128 you minimize the size of shift register needed and the number of wires needed for parallel transmissions.

Conclusion

24. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan A. Dare
July 24, 2006

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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